REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - ro	02-01-07	R. MONNIN

REV																				
SHEET																				
REV	A																			
SHEET	15																			

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
MICHAEL FRYE

DRAWING APPROVAL DATE
95-11-15

MICROCIRCUIT, LINEAR, DUAL, 12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-94518**

SHEET 1 OF 15

DSCC FORM 2233
APR 97

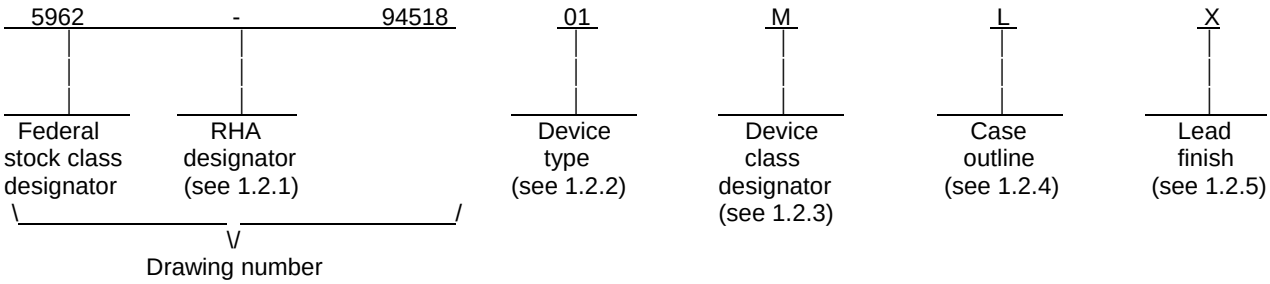
5962-E132-02

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7837	Dual, 12-bit multiplying digital-to-analog converter
02	AD7847	Dual, 12-bit multiplying digital-to-analog converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{DD} to DGND, AGNDA, AGNDB ..... -0.3 V to +17 V
V_{SS} to DGND, AGNDA, AGNDB ..... -0.3 V to –17 V 2/
V_{REFA}, V_{REFB} to AGNDA, AGNDB ..... V_{SS} –0.3 V to V_{DD} +0.3 V
AGNDA, AGNDB to DGND ..... -0.3 V to V_{DD} +0.3 V
V_{OUTA}, V_{OUTB} to AGNDA, AGNDB ..... V_{SS} –0.3 V to V_{DD} +0.3 V 3/
R_{FBA}, R_{FBB} to AGNDA, AGNDB ..... V_{SS} –0.3 V to V_{DD} +0.3 V 4/
Digital inputs to DGND ..... -0.3 V to V_{DD} +0.3 V
Power dissipation (P_D) to +75°C ..... 1000 mW 5/
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Positive supply voltage (V_{DD}) ..... +15 V
Negative supply voltage (V_{SS}) ..... -15 V
Ambient temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If V_{SS} is open circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive, exceeding the absolute maximum ratings. If the possibility exist, Schottky diode connected between V_{SS} and AGND (cathode to AGND) ensures the maximum rating will be observed.
3/ The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.
4/ Device type 01 only.
5/ Derates above T_A = +75°C at 10 mW/°C.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagrams. The block diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES		1,2,3	All		12	Bits
Relative accuracy	RA		1,2,3	All		±1	LSB
Differential nonlinearity	DNL		1,2,3	All		±1	LSB
Zero code offset error	ZCOE	DAC latch loaded with all 0's	1	All		±2	mV
		t_{COE} = ±5 µV/°C	2,3			±5	
Gain error	GE	DAC latch loaded with all 1's	1	All		±5	LSB
		t_{COE} = ±2 ppm of FSR/°C	2,3			±7	
Input high voltage	V_{INH}		1,2,3	All	2.4		V
Input low voltage	V_{INL}		1,2,3	All		0.8	V
Input current	I_{IN}	Digital inputs at 0 V and V_{DD}	1,2,3	All		±1	µA
Positive supply voltage range	V_{DD}		1,2,3	All	14.75	15.75	V
Negative supply voltage range	V_{SS}		1,2,3	All	-14.75	-15.75	V
Power supply rejection ratio	+PSRR	V_{DD} = +14.25 to +15.75 V, V_{REF} = -10 V	1,2,3	All		±0.1	%
	-PSRR	V_{SS} = -14.25 to -15.75 V, V_{REF} = +10 V				±0.1	
Positive supply current	I_{DD}	Output unloaded	1,2,3	All		10	mA
Negative supply current	I_{SS}	Output unloaded	1,2,3	All		6	mA
V_{REF} input resistance	R_{VIN}		1,2,3	All	8	13	kΩ
V_{REFA}, V_{REFB} resistance matching	RM		1,2,3	All		±3	%
Input capacitance	C_{IN}	T_A = +25°C 2/	4	All		8	pF
Functional test		See 4.4.1b	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{CS}$ to $\overline{WR}$ setup time	t_1	3/ 4/	9,10,11	All	0		ns
$\overline{CS}$ to $\overline{WR}$ hold time	t_2	3/ 4/	9,10,11	All	0		ns
$\overline{WR}$ pulse width	t_3	3/ 4/	9	All	80		ns
			10,11		100		
Data valid to $\overline{WR}$ setup time	t_4	3/ 4/	9,10,11	All	80		ns
Data valid to $\overline{WR}$ hold time	t_5	3/ 4/	9,10,11	All	10		ns
Address to $\overline{WR}$ setup time	t_6	3/ 4/	9,10,11	All	15		ns
Address to $\overline{WR}$ hold time	t_7	3/ 4/	9,10,11	All	15		ns
$\overline{LDAC}$ pulse width	t_8	3/ 4/	9	All	80		ns
			10,11		100		

1/ Unless otherwise specified, V_{DD} = +15 V, V_{SS} = -15 V, AGNDA = AGNDB = DGND = 0 V, V_{REFA} = V_{REFB} = +10 V, R_L = 2 kΩ, and C_L = 100 pF. For device type 01, V_{OUT} is connected to R_{FB}.

2/ If not tested, shall be guaranteed to the limits specified in table I herein

3/ All input signals are specified with t_R = t_F = 5 ns (10% to 90% of 5 V) and timed from a voltage from a voltage level of 1.6 V.

4/ See figure 4.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

Device types	01	02
Case outline	L	
Terminal number	Terminal symbol	
1	$\overline{CS}$	$\overline{CSA}$
2	R_{FBA}	$\overline{CSB}$
3	V_{REFA}	V_{REFA}
4	V_{OUTA}	V_{OUTA}
5	AGNDA	AGNDA
6	V_{DD}	V_{DD}
7	V_{SS}	V_{SS}
8	AGNDB	AGNDB
9	V_{OUTB}	V_{OUTB}
10	V_{REFB}	V_{REFB}
11	DGND	DGND
12	R_{FBB}	DB11
13	$\overline{WR}$	$\overline{WR}$
14	$\overline{LDAC}$	DB10
15	A1	DB9
16	A2	DB8
17	DB7	DB7
18	DB6	DB6
19	DB5	DB5
20	DB4	DB4
21	DB3	DB3
22	DB2	DB2
23	DB1	DB1
24	DB0	DB0

FIGURE 1. Terminal connections.

Device types 01 and 02

Terminal symbol	Description
V_{REFA}	Reference input voltage for DAC A. This may be an ac or dc signal.
V_{OUTA}	Analog output voltage from DAC A.
AGNDA	Analog ground for DAC A.
V_{DD}	Positive power supply.
V_{SS}	Negative power supply.
AGNDB	Analog ground for DAC B.
V_{OUTB}	Analog output voltage from DAC B
V_{REFB}	Reference input voltage for DAC B. This may be an ac or dc signal.
DGND	Digital ground. Ground reference for digital circuitry.

Device type 01 only

Terminal symbol	Description
$\overline{CS}$	Chip select. Active low logic input. The device is selected when this input is active.
R_{FBA}	Amplifier feedback resistor for DAC A.
R_{FBB}	Amplifier feedback resistor for DAC B.
$\overline{WR}$	Write input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
$\overline{LDAC}$	DAC update logic input. Data is transferred from the input latches to the DAC latches when $\overline{LDAC}$ is taken low.
A1	Address input. Most significant address input for input latches.
A0	Address input. Least significant address input for input latches.
DB7 – DB4	Data bit 7 to data bit 4.
DB3 – DB0	Data bit 3 to data bit 0 (LSB) or data bit 11 (MSB) to data bit 8.

Device type 02 only

Terminal symbol	Description
$\overline{CSA}$	Chip select input for DAC A. Active low logic input. DAC A is selected when this input is low.
$\overline{CSB}$	Chip select input for DAC B. Active low logic input. DAC B is selected when this input is low.
DB11	Data bit 11 (MSB).
$\overline{WR}$	Write input. $\overline{WR}$ is a positive edge triggered input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
DB10 - DB0	Data bit 10 to data bit 0 (LSB).

FIGURE 1. Terminal connections – continued.

Device type 01

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No data transfer
X	1	X	X	1	No data transfer
0	0	0	0	1	DAC A LS input latch transparent
0	0	0	1	1	DAC A MS input latch transparent
0	0	1	0	1	DAC B LS input latch transparent
0	0	1	1	1	DAC B MS input latch transparent
1	1	X	X	0	DAC A and DAC B latches updated simultaneously from the respective input latches

Device type 02

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No data transfer
1	1	X	No data transfer
0	1	↑	Data latched to DAC A
1	0	↑	Data latched to DAC B
0	0	↑	Data latched to both DAC's
↑	1	0	Data latched to DAC A
↑	↑	0	Data latched to DAC B
↑	↑	0	Data latched to both DAC's

FIGURE 2. Truth table.

Device type 01

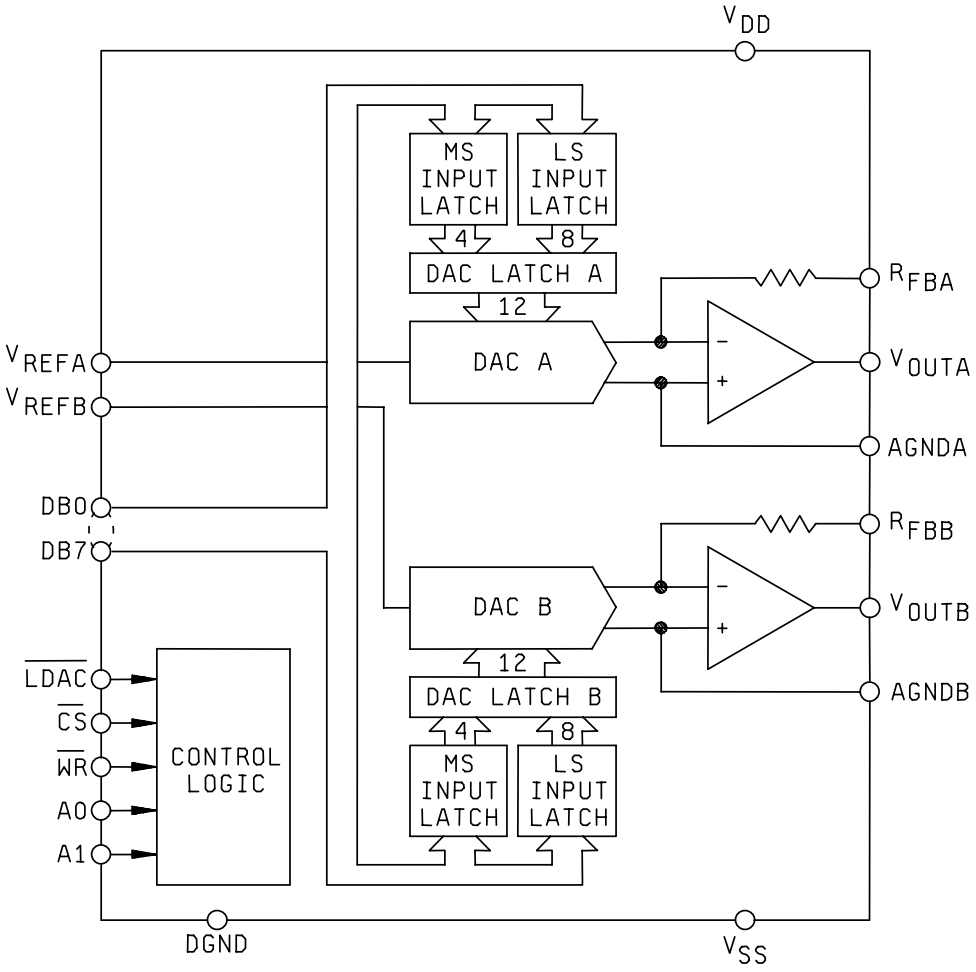


FIGURE 3. Block diagram.

Device type 02

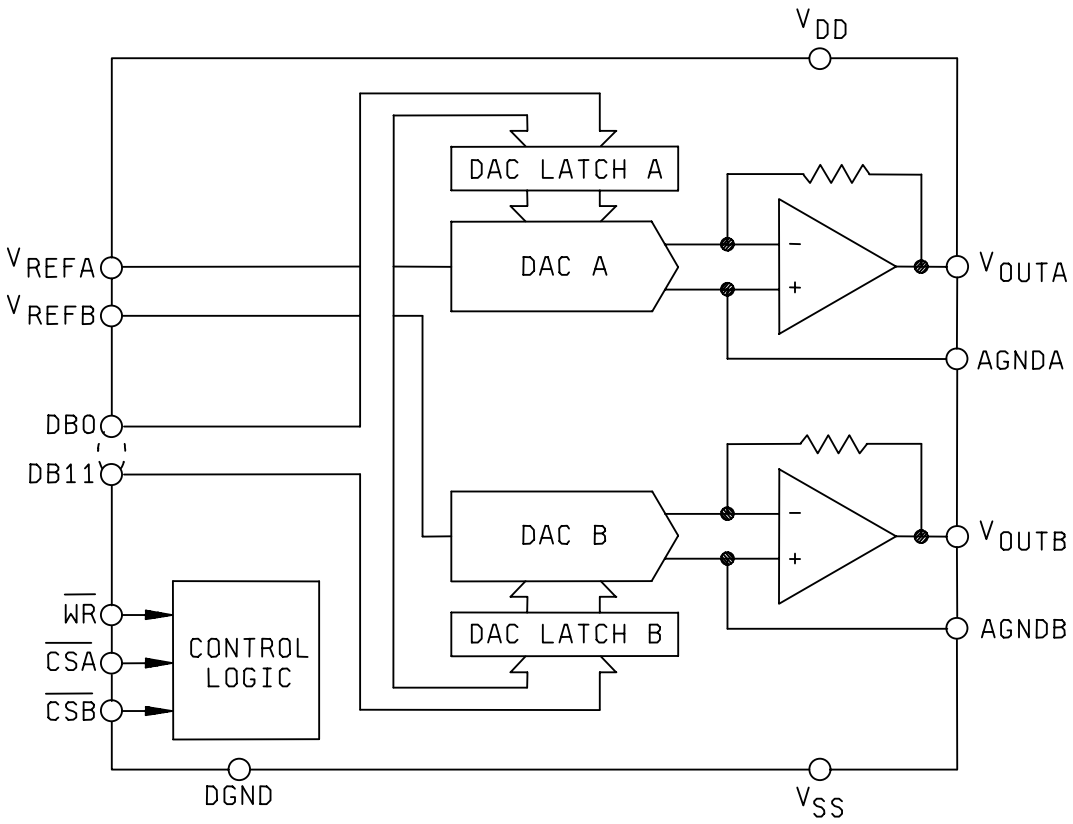


FIGURE 3. Block diagram – Continued.

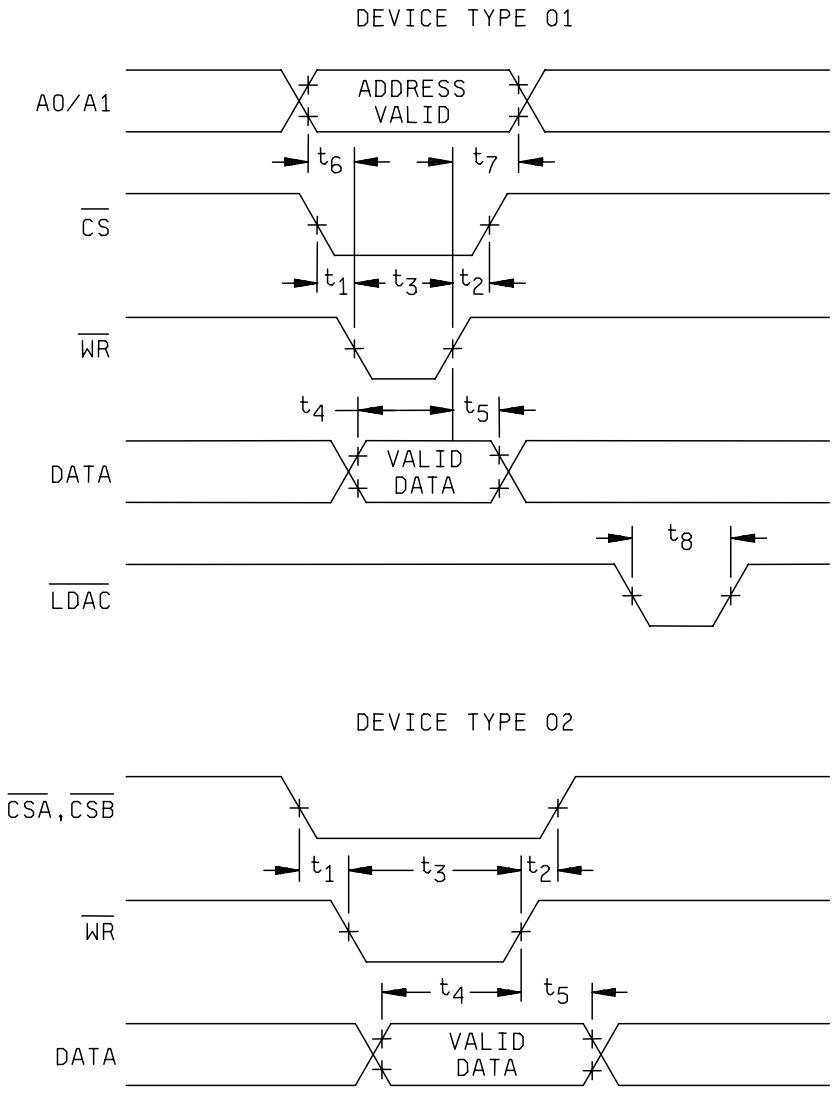


FIGURE 4. Timing waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,9,10,11 1/	1,2,3,9, 1/ 10,11	1,2,3,9, 1/ 10,11
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8, 9,10,11	1,2,3,4,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-01-07

Approved sources of supply for SMD 5962-94518 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9451801MLA	24355	AD7837SQ/883B
5962-9451802MLA	24355	AD7847SQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Bay F-1 Raheen Ind. Estate Limerick, Ireland

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